Kirk Weedman

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Design Engineer with a proven track record to define and develop systems (boards, SoC FPGAs both large and small, etc.) to client hardware and software specifications as well as creation of specifications and documentation. Proven designer of Verilog RTL and behavioral designs, synthesis, place & route, functional testing and debugging. Designer of C/assembly firmware that interfaces to the RTL Verilog designs. Ability to work entirely alone, with others (both H/W and/or S/W), or as a HW lead.

EXPERIENCE:

HDL Express: Creating a new Out of Order CPU architecture that may improve IPC in modern CPUs. This new method does not use the Tomasulo algorithm, but a new method that effectively does the same but without the complications. Currently using an ARMv7 ISA for testing. Using SystemVerilog and ModelSim for design/debugging

Created a new pipelined CPU architect to demonstrate a new method I've invented (working on patent) called "A Novel Concept to Eliminate Branch Misprediction in Pipelined CPU's". This method is working in simulation as of Jan. 2016. The emphasis here is that it eliminates mispredictions – not minimizes mispredictions. Also working on testing the method in an new OoOE CPU I'm designing.

InnovAsic: March/April 2015 - Created FPGA logic to do SIMON encryption/decryption of Ethernet packet data.

HDL Express: Oct 2014 - March 2015

Learning to use Xilinx Platform Studio to integrate Xilinx peripherals with a MicroBlaze CPU as well as setting up the SDK. Designing a new C compiler to work with various FPGA CPUs including my own cpu designs.

Ossia: Redmond, WA Oct. 2012 – Oct 2014

Design, simulation, test bench creation & verification, debugging, etc. of two different Xilinx Spartan 6 FPGAs. Design included I2C, SPI, and a custom serial comm. over M-LVDS with up to 32 drops with bi-dir comm. between the FPGAs as well as many other types of custom state machines, logic & IP for the FPGAs. For one of the FPGAs I designed a custom 16 bit Harvard type arch. CPU/Microcontroller with one of the FPGAs running 32 instances of it. Also designed/wrote an assembler for the CPU (with high level extensions such as nested IF/ELSE, WHILE) using Flex/Bison. Used ModelSim 10.1c, Xilinx ISE 14.7, Flex & Bison, C low level interface (to FPGA) programming, as well as using the custom assembler I created to design the code used on the custom CPU in the FPGA. Also briefly used Microsemi FPGA tools and Xojo devel.

Western Digital: Longmont, CO April & May, 2012

Helped bring up a new Cadence Rapid Prototyping Platform for hardware based simulation/acceleration.

Microsoft: Redmond, WA July 2010 – Aug 12, 2011

See www.surface.com Verilog FPGA design/RTL, debugging and test. Design included on screen display graphics overlay as well as temporal and ambient correction of the "pixel sense", I2C, SPI, and custom interfaces. Debugging and test included many changes/fixes to all areas of code. This design was for a Xilinx Spartan 6. Tools: Xilinx ISE 13.1, Blue Pearl Verilog analysis tools, Chipscope, Microsoft Source Depot Browser, and QuestaSim.

www.OPENHPSDR.ORG Nov 2008 – April 2010

see http://openhpsdr.org/wiki/index.php?title=HPSDRwiki:Community_Portal

and http://openhpsdr.org/wiki/index.php?title=Verilog

- Verilog RTL & Behavior design, synthesis, simulation, timing analysis/closure, place & route, functional verification and debugging for a software defined radio (0 - 61 MHz)
- Altera Quartus 8.0/8.1/9.0, ModelSimSE 6.4, Tortoise SVN version control for code backup. etc.
- I/Q data generation using a cordic algorithm and N stage Decimating CIC filters in Verilog RTL
- Verilog RTL I2S data transfers design, multiple clock domains. FIFO IP integration for data transfers between domains. Also teaching a Verilog course. See verilog.openhpsdr.org to download my class videos, etc..

Teseda Portland, Oregon. Jan 2003 - Feb 2008

Title: Senior Hardware Design Engineer

FPGA Design: Responsible for all large FPGA designs from architect, design, simulation, etc.. to production

- Verilog RTL & Behavioral design, synthesis, timing analysis/closure, place & route, functional verification and debugging for a new DFT Tester
- Multiple clock domain designs – without metastability & CDC (clock domain crossing) issues
- DDR2 (216 bit wide) IP integration with a memory interface at 200Mhz
- 400Mhz I/O using DDR flops
- Virtex 2, 4, & 5 design/debugging experience - Xilinx XC2V200 & XC5VLX110 FPGA designs in Verilog RTL code.
- ModelSimSE 6.1, Xilinx ISE versions 6 - 10.1 & Chipscope experience
- FPGA DLL based designs

Contract Engineering work. March 2001 – Dec 2002

Title: Contract Design Engineer

- Taught Verilog language classes to Nortel engineers in Ottawa Canada.
- Verilog RTL & Behavioral design for Teseda (a new startup company) – see above.

Xerox/Tektronix Inc., Wilsonville, Oregon. April 1992 - March 2001

Title: Senior Hardware/Software Design Engineer

FPGA Design:

Responsibilities:

- RTL & Behavioral Verilog code for FPGA & ASIC designs.
- Verilog Functional Simulation/Verification of designs.
- Post-layout (back-annotated) Verilog simulation & timing analysis/closure
- PCB design to support FPGA or ASIC development.
- Conversion of FPGAs to ASICs.
- Detailed Register Level documentation of FPGAs or ASICs

Hardware Design:

- Board-level design and electrical specifications.
- Design of RISC based microprocessor controllers
- Cadence tools for design entry under Sun UNIX OS.
- Design, validation and test of printed circuit boards.
- Coordinated engineers in design projects.

Firmware Design

- Low level software drivers, 8 bit embedded firmware & low level drivers

EMC:

- EMC testing and certification for CISPR22 and FCC B. PCB design for EMC compliance.

Various tools used: Cadence Verilog XL, Cadence Concept, Synopsis, Synplicity, Altera MaxplusII, Xilinx, Atmel AVR, various Microprocessors, etc.

Mannesmann Tally, Kent WA 1/88 - 4/92

Responsibility:

- Co-design of an ASIC. Hardware Logic/State Machine Design – PALS and in RTL for ASIC.
- RTL Synthesis, Simulation, Test and Verification of part of an ASIC. Design of Microprocessor based Printer Controller.

Telex Computer Products Tulsa, OK 1/87 - 12/87

- Token Ring Support Software – C and 80x86 assembly. Taught C Programming Class at Tulsa Junior College.

Flight Safety International Tulsa, OK 5/84 - 1/87

- Wrote Simulation S/W for an aircraft simulator using C & 68000 Assembly Language, Design, Modeling and Simulation SW (C & 68K assembly) for a Radar Simulator. Designed a 68000 based personal computer including BIOS and I/O drivers for CPM 68K OS.

Teltronics Lakeland, FL 2/83 - 5/84

- Designed a tone-to-pulse converter for use in telephone central office. Analog audio filter designs – passive & active designs

References: available on request

Additional Information:

- **Job title**: Engineering - Hardware / Software
  Years of experience: 30+
  Education Level: BSEE – Walla Walla University 1983
  Relocation: as needed at no cost
  Citizenship: United States